IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of Chung-Hui Chen

Serial No.: 10/791,044 Art Unit: 2816

Filed: March 1, 2004 Examiner: Long T. Nguyen

Title: DOUBLE-EDGE-TRIGGER FLIP-FLOP

Reasons Accompanying Pre-Appeal Brief Request for Review

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Commissioner for Patents
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Alexandria, VA 22313-1450

Sir:

As noted in the Final Office Action mailed March 10, 2006, claims 1-13, 15-18 and 20-24 are pending and stand rejected. Specifically, claims 1-13, 15-18 and 20 stand rejected for containing various informalities. In addition, the same claims are rejected as allegedly anticipated by Patent No. 5,081,373 to Suzuki.

To expedite the pre-appeal conference, Applicant's counsel telephonically discussed the Examiner's formal objections with SPE Callahan on June 19, 2006. SPE Callahan suggested that the formal objections be held at abeyance pending the outcome of the pre-appeal conference. Accordingly, this communication will only address the substantive issues.

A. Anticipation over Suzuki

The Examiner alleges that the Suzuki reference anticipates each of the independent claims 1, 7, 12, 15, and 21-24. Applicant respectfully disagrees with the ground of this rejection.

The claimed invention is directed to a fast double-edge-trigger flip-flop. Conventional flip-flops store s logical state in response to a clock pulse and one or more input data signal. Flip-flops operate in selected sequences by capturing and retaining data for the other circuits within the system. In this manner, sequential logic circuits operate to capture, store and transfer data during successive clock signals. A double edge flip-flop latches and holds the logical state of its data input at both the rising and the falling edge of its clock input. Conventional flip-flops use cross-coupled inverters which are slow and inaccurate. The claimed embodiments overcome these and other deficiencies.

By way of example, independent claim 1 is directed to a double-edge flip-flop having, among others, a first signal passing module (308 in Fig. 1) and a second passing module (310). At least one of the first or the second passing module can be NAND gate. Further, the input to the NAND gate (308, 310) is a flag signal (312) and a data signal (304, 306). The data signal (304, 306) for each NAND gate (308, 310) is an output of a pass-gate (SW0, SW1) associated each respective NAND gate. Each of the remaining independent claims includes a similar recitation.

The reference to Suzuki does not disclose nor suggest such a NAND gate, much less a NAND gate having the same inputs (*i.e.*, a flag signal and a data signal) as recited in the claims. Suzuki is directed to a circuit for sampling digital data. The Examiner relies on Fig. 1 of Suzuki and alleges that a combination of AND gate 131 and inverter 141 is a NAND gate (See Office Action at page 3.) The Examiner's conclusion is inaccurate for several reasons.

First, elements 141 and 142 of Suzuki are NOR gates, with RST signal inputs, not inverters as stated. Whether or not the RST signal is used, components 141 and 142 will act as NOR gates. Therefore, Suzuki does not contain the same elements as claims 1, 7, 12, 15 or 21-24 and cannot properly anticipate them.

Second, combining an AND gate and a NOR gate neither produces the same output as, nor includes the same components as a NAND gate. In other words, a combination of an AND gate and a NOR gate is not the functional equivalent of a NAND gate. A NAND gate is a single device and therefore requires fewer components than an AND gate combined with a NOR gate. Therefore, using a single NAND gate provides the advantages of lower costs and higher efficiency over combining an AND gate and a NOR gate.

Third, as amended herein, the NAND gate of independent claims 1, 7, 12, 15 and 21-24 includes a flag signal input. This flag signal is functionally different from the preset PST and reset RST signal inputs of Suzuki. "[T]he flag identifies the power status of the circuit to prevent leakage problems when the flip-flop is not in operation," [Paragraph 0011]. By comparison, the PST signal is used to initialize the signal passing portion (Col. 5, lines 32-33) and the reset signal is used to clear the hold data of the signal passing portion (Col 5, Line 32-35). Therefore, because Suzuki neither discloses nor implies a flag signal, Suzuki can not anticipate Applicant's independent claims.

B. Obviousness Rejection over Suzuki

Claims 5-6, 10-13, 20 and 23 stand rejected as allegedly obvious over Suzuki in vie of Weste *et al.* (Principles of CMOS VLSI Design: A Systems Perspective, 1993, Addison-Wesley Publ'g Co., 2nd ed, page 91).

Each of claims 5-6, 10-11, 13 and 20 depends from an otherwise patentable claim and is deemed patentable at least by the virtue of this dependence. Accordingly, additional reasons for patentability of each of these claims will not be proffered.

Independent claim 12 recites, among others, "wherein at least one of the first or the second signal passing module is a NAND gate; and wherein each NAND gate receives a flag signal together with the respective passing input of the associated pass gate wherein the flag signal disables the flip-flop when the flag signal is asserted". Independent claim 23 recites, among others, "wherein each of the first signal passing module and the second signal passing module is a NAND gate for receiving a flag signal together with the respective passed input of the first and the second pass gate." Suzuki fails to disclose or suggest at least these elements of each claim. The Examine has not explained, and Applicant cannot determine, how the secondary reference to Weste addresses these deficiencies.

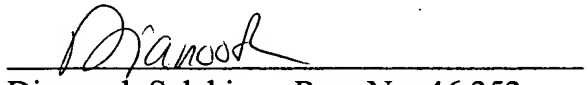
Moreover, Suzuki *teaches away* from using a single NAND gate and a flag signal and requires instead a PST and RST signal. Additionally, West *et al.* discloses only a method of construction of tristate inverters. Therefore, claims 5, 6, 10-14 and 20-23 can not be obvious over Suzuki in view of West *et al.*

Therefore, Applicant respectfully submits that the a *prima facie* case of obviousness has not been established.

CONCLUSION

In summary, the anticipation rejection over Suzuki is improper because, among others, the reference does not disclose a NAND gate receiving a flag signal and a data signal as claimed in each independent claim. Each of these components are adequately defined in Applicant disclosure. The obviousness rejection of dependent claims 12 and 23 is equally improper because the Office has not established a *prima facie* case of obviousness by showing how the secondary reference addresses Suzuki's deficiencies. The dependent claims are deemed patentable at least by the virtue of their dependence on otherwise allowable claims.

Respectfully submitted,



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